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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,305	04/16/2004	Kenya Ishii	119342	7761

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
09/10/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/825,305	ISHII, KENYA	
	Examiner	Art Unit	
	STEPHEN G. SHERMAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/16/2004; 10/19/2006; 10/16/2007; 1/15/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the application filed 16 April 2004. Claims 1-14 are pending.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on 16 April 2004, 19 October 2006, 16 October 2007 and 15 January 2009 are being considered by the examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-6, 8 and 10-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishii (JP 11-119,746 A).

Regarding claim 1, Ishii discloses an electro-optical panel driving circuit, comprising:

a substrate (Paragraphs [0007], [0038] and [0041]);

pixel electrodes provided above the substrate (Paragraphs [0006] and [0038] and Drawing 4);

switching elements that switch on and off the corresponding pixel electrodes (Drawing 4, 114 and paragraphs [0006] and [0038]);

data lines that supply image signals to the corresponding pixel electrodes via the corresponding switching elements (Drawing 4, 112a-g and paragraphs [0005] and [0038]);

a shift register circuit that sequentially outputs transfer signals (Drawing 8, 120, 130, 140 and 150 and paragraphs [0012] and [0038]);

a buffer circuit that buffers the sequentially output transfer signals (Drawing 8, 160a-f and 162a-f and paragraphs [0021] and [0038]);

a sampling circuit that samples the image signals using the buffered transfer signals as sampling pulses and that supplies the sampled image signals to the corresponding data lines (Drawing 8, 106a-f and paragraphs [0022] and [0038]); and

a dummy circuit that simulates at least part of the buffer circuit and the sampling circuit (Drawing 1, 27 and paragraph [0041]),

delay signals indicating the amount of delay of the sampling pulses and generated by the dummy circuit being fed back to the shift register circuit so that the amount of delay is reduced (Drawings 1 and 8 and paragraphs [0049]-[0053]), and

the buffer circuit, the sampling circuit, and the dummy circuit provided on the substrate (Paragraphs [0041] and [0043]).

Regarding claim 3, Ishii discloses the electro-optical panel driving circuit according to Claim 1,

the buffer circuit including a plurality of stages of buffers connected in series (Drawing 8, 160a-f and 162a-f),

the sampling circuit including analog sampling switches (Drawing 8, 106a-f), and

the dummy circuit simulates at least the buffer in the final stage among the plurality of stages of buffers (Drawing 1).

Regarding claim 4, Ishii discloses the electro-optical panel driving circuit according to Claim 3, the dummy circuit simulates the sampling switches and all of the plurality of stages of buffers (Drawing 1 and paragraph [0054]).

Regarding claim 5, Ishii discloses the electro-optical panel driving circuit according to Claim 1, semiconductor elements constituting the sampling circuit formed in the same process and at the same time as semiconductor elements constituting the corresponding dummy circuit (Paragraph [0042]).

Regarding claim 6, Ishii discloses the electro-optical panel driving circuit according to Claim 5, each of the semiconductor elements is an N-type semiconductor element (Drawings 1 and 8).

Regarding claim 8, Ishii discloses the electro-optical panel driving circuit according to Claim 1, further comprising:

a timing adjusting circuit (Drawing 1, 21, 22, 23, 25 and 26),

the shift register circuit sequentially outputting the transfer signals in accordance with a clock cycle of clock signals (Drawings 1, 8 and 10), and

the timing adjusting circuit adjusting the timing of the clock signals input to the shift register circuit on the basis of the amount of delay indicated by the delay signals (Drawing 10 and paragraphs [0049]-[0053]).

Regarding claim 10, Ishii discloses the electro-optical panel driving circuit according to Claim 1, the channel width of first thin-film transistors constituting the sampling circuit equal to the channel width of second thin-film transistors constituting the dummy circuit, the second thin-film transistors corresponding to the first thin-film transistors (Paragraph [0042]).

Regarding claim 11, Ishii discloses the electro-optical panel driving circuit according to Claim 1,

the channel width of second thin-film transistors constituting the dummy circuit, the second thin-film transistors corresponding to first thin-film transistors constituting the sampling circuit, being smaller than or equal to the channel width of the first thin-film transistors (Paragraph [0042]), and

the ratio of the size of the first thin-film transistors to the size of a first buffer circuit in the preceding stage of the first thin-film transistors being equal to the ratio of the size of the second thin-film transistors of the dummy circuit to the size of a second buffer circuit in the preceding stage of the second thin-film transistors (Paragraph [0042]).

Regarding claim 12, Ishii discloses the electro-optical panel driving circuit according to Claim 1,

the buffer circuit including a plurality of stages of buffers connected in series (Drawing 8, 160a-f and 162a-f),

the sampling circuit including analog sampling switches (Drawing 8, 106a-f),

the channel width of second thin-film transistors constituting the dummy circuit, the second thin-film transistors corresponding to first thin-film transistors functioning as the sampling switches, being smaller than or equal to the channel width of the first thin-film transistors (Paragraph [0042]), and

the ratio of the size of the first thin-film transistors to the size of the buffer in the final stage of the first buffer circuit in the preceding stage of the first thin-film transistors being equal to the ratio of the size of the second thin-film transistors of the dummy

circuit to the size of the buffer in the final stage of a second buffer circuit in the preceding stage of the second thin-film transistors (Paragraph [0042]).

Regarding claim 13, Ishii discloses an electro-optical device comprising the electro-optical panel driving circuit as set forth in Claim 1 and the electro-optical panel driven by the driving circuit (Drawings 2 and 3).

Regarding claim 14, Ishii discloses an electronic apparatus, comprising: the electro-optical device as set forth in Claim 13 (Drawings 2 and 3).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 11-119,746 A).

Regarding claim 2, Ishii discloses the electro-optical panel driving circuit according to Claim 1.

Ishii fails to explicitly teach that the shift register circuit provided in an integrated circuit externally attached to the substrate, however, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to separate the shift register from the substrate since it is not described as being essential to the Applicant's invention, and because it was determined to require only routine skill in the art to make elements separable and is a matter of obvious engineering choice. *Nerwin v. Erlichman, 168 USPQ 177. In re Dulberg, 289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961)*. See MPEP 2144.04.

Regarding claim 9, this claim is rejected under the same rationale as claim 2.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 11-119746 A) in view of Ito et al. (JP 02-142326 A).

Regarding claim 7, Ishii discloses the electro-optical panel driving circuit according to Claim 5, further comprising:

a timing adjusting circuit (Drawing 1, 21, 22, 23, 25 and 26),

each of the semiconductor elements being a thin-film transistor (Figure 1, 275 and paragraph [0042]),

the shift register circuit sequentially outputting the transfer signals in accordance with a clock cycle of clock signals (Drawings 1, 8 and 10), and

the timing adjusting circuit adjusting the timing of the clock signals input to the shift register circuit on the basis of the timing of the falling edge of the delay signals detected by the detection terminal (Drawing 10).

Ishii fails to teach that the source of the thin-film transistor connected to a low-potential power supply of the driving circuit and the drain of the thin-film transistor biased at a high-potential power supply of the driving circuit and connected to a detection terminal of the driving circuit.

Ito et al. disclose of a source of a thin-film transistor connected to a low-potential power supply and the drain of the thin-film transistor biased at a high-potential power supply and connected to a detection terminal (Drawing 1 shows that the source of TFT 2 is connected to ground while the drain of TFT 2 is biased at voltage 6 and connected to a detection terminal Vout.).

Therefore, it would have been obvious to “one of ordinary skill” in the art at the time the invention was made to use the teachings of Ito et al. in the dummy circuit taught by Ishii in order to better regulate the detection and voltage output of the circuit.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Uchino et al. (US 5,959,600) discloses a display device data driving circuit having a shift register, a buffer circuit and a sampling circuit.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN G. SHERMAN whose telephone number is (571)272-2941. The examiner can normally be reached on M-F, 7:30 a.m. - 4:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen G Sherman/
Examiner, Art Unit 2629

7 September 2010